Analog Electronics Neural Networks: Analog Computing combined with Digital Data Processing Revisited

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Introduction

From 5000 BC - 1900 AC: Analog Calculations using Mathematics and intelligent human brains

From 1920 AC - TODAY: Digital Computation using Electronics

From 1873 AC - 1970: Analog Computation using Mechanics and Electronics

From 2020 AC - FUTURE?: Analog Computation revisited using printed Electronics?

Digital Computation bases on discretized binary digital logic, Analog Computation bases on continuous difference amplifiers (Operational Amplifier)!

Introduction

Fig. 1. An Analog Computer: Polish analog computer AKAT-1, from 1959

Introduction

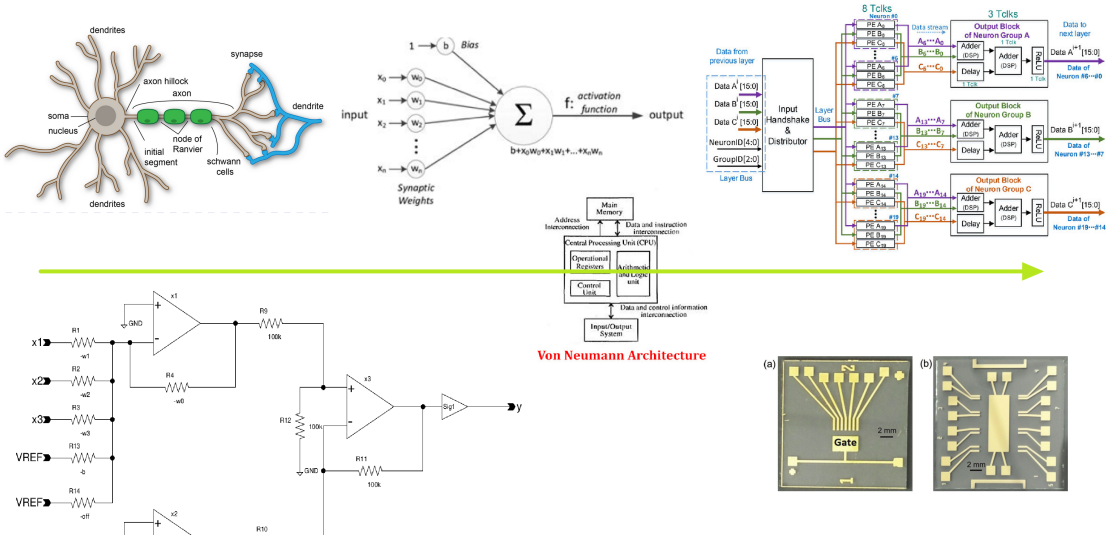


Fig. 2. Evolution of Neural Networks: Bio Analog - Mathematical - E-Digital - E-Analog & Printed?

Motivation

Arguments against digital systems:

1. Digital computations introduces numerical discretization and rounding errors that can be significant for highly non-linear functional networks;
2. Transistor resource demand and constraints:
   - Digital logic: ANN with 10 nodes requires more than 1000 transistors
   - Computer logic: Resources independent from problem size; about 1E6-1E10 transistors!
   - Analog electronics: ANN with 10 nodes requires at least 120 transistors (as shown in this work)
3. Electrical power requirements and constraints:
   - Digital logic: about 1-10 mW
   - Computer logic: about 100 mW-100 W
   - Analog electronics: below 1 mW
4. Robustness and safety?
5. Printed Eöectronics - a key enabler technology, but still challenging and not suitable for large (digital) circuits (below 100 transistors)

Long- and short-term Goals

1. Implementation of digital algorithms with analog electronics
2. Analog computational circuits as a co-working system in a mixed analog-digital system
3. Analog computational circuits as a replacement for digital computation with pure analog systems
4. New design methodologies
   - Scaling and transformation algorithms (from digital to analog circuits)
   - Training of parametrizable analog models
   - Functional design of electronic circuits with probabilistic methods (e.e.g, evolutionary algorithms)
   - Simulation-in-the-loop algorithms
   - Parametrizable hardware-in-the-loop methods

Applications

- Signal pre- and post-processing
  - Frequency filters
  - Integration
  - Wavelet decomposition using filter banks
  - Signal hull generation (analytical signal transformation)
  - Frequency decomposition (Fourier transform)?
  - Correlation?
- Function regression
- **Artificial Neural Networks (e.g., damage predictors)**
- Machine Control
- Rapid prototyping with field-programmable computers
  - SoC Digital logic: Yes, available (FPGA)!
  - SoC Analog circuits: Maybe (FPAA), Not suitable?
  - Discrete Matrix Analog circuits with AD interface: Not yet available, but Yes suitable

Applications

Material-integrated Intelligent Systems

[https://arxiv.org/pdf/2302.09002]

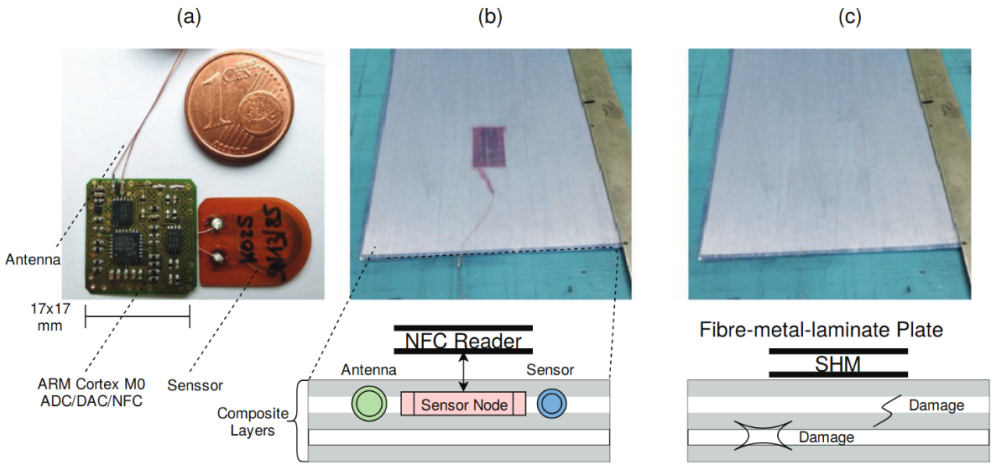


Fig. 3. Highly miniaturized sensor node (Lüssem et al.,IMSAS, Uni. Bremen)

Pro-Cons

Digital Circuits

[+] High signal(information)-to-noise ratio, noise immunity
[-] Discretization errors
[-] High transistor count (TC)
[-] High(er) power consumption

Analog Circuits

[+] No discretization errors
[+] Lowest power
[+] Lowest TC
[-] Lower SNR
[-] Noise, noise sensitivity...

Accuracy versa Precision!

Accuracy versa Precision

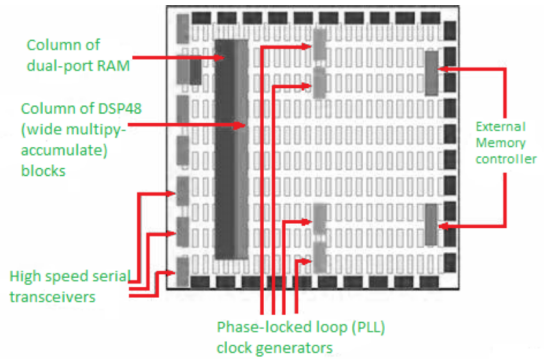
Accuracy refers primarily to the relationship between a simulation and the primary system it is simulating or, more generally, to the relationship between the results of a computation and the mathematically correct result.

Accuracy is a result of many factors, including the mathematical model chosen, the way it is set up on a computer, and the precision of the analog computing devices.

Precision,is a narrower notion, which refers to the quality of a representation or computing device. In analog computing, precision depends on resolution (fineness of operation) and stability (absence of drift) and may be measured as a fraction of the represented value

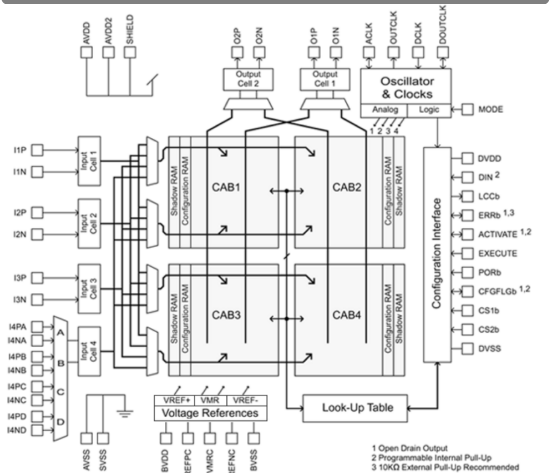
Implementations

Field Programmable Gate Array



Digital circuits, look-up tables, flip-flops's, programmable switches, DSP

Field Programmable Analog Array



Switched Capacitor Blocks and Matrix Switch

Analog Computation versa Digital Signalprocessing

DSP is mainly signal processing in time and frequency domains. Analog Computation is more general and includes DSP as a sub-set.

- The Field Programmable Analog Array (FPAA) technologies focus on signal pre-processing.
- Complex computation (e.g., solving equations or computation of neural networks) is not possible with FPAA - too limited architecture.
- So the FPAA technologies rised in 2015-2022, but now vanishes again!
- In contrast, FPGA sattled in the digital market even for general purpose solutions including processor designs.
- **FPAAs are not Analog Computers (as built in the 1940-1960's)**

History

[Ulmann, 2013]

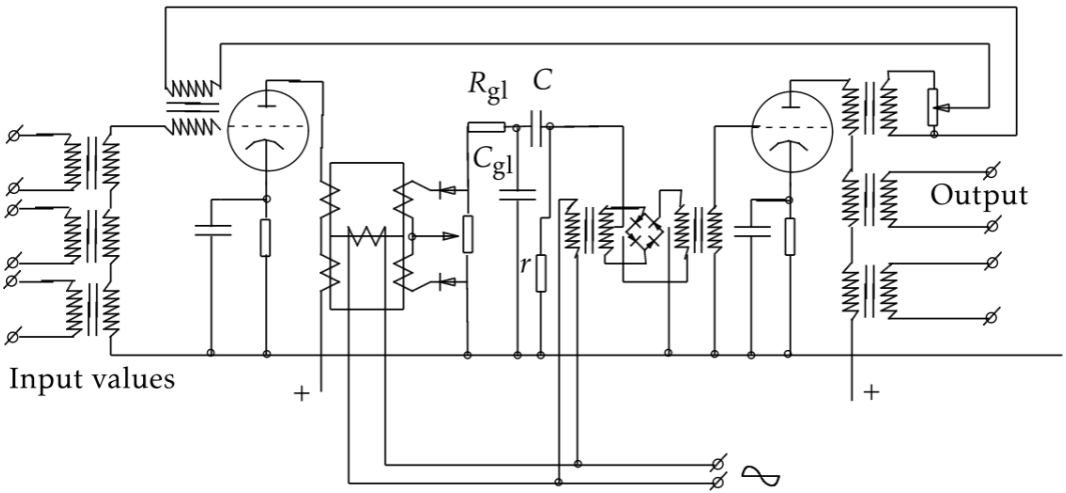


Fig. 4. 1946: Hoelzer's differentiator circuit - well okay it performs analog computations

History

[Ulmann, 2013]

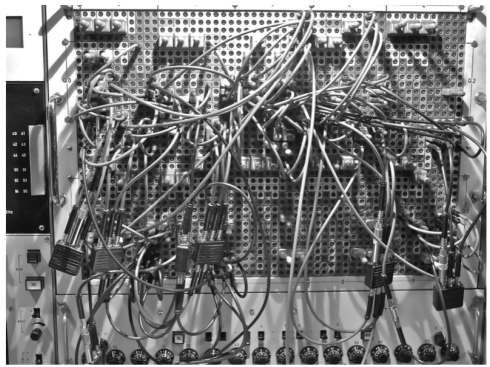


Fig. 5. (Left) 1946: Hoelzer's differentiator machine (Right) Programming of AC - far beyond what we want

Main applications were solving differential equations using differentiators, integrators, or a composed circuits of differentiator and integrator circuits

[Ulmann, 2013]

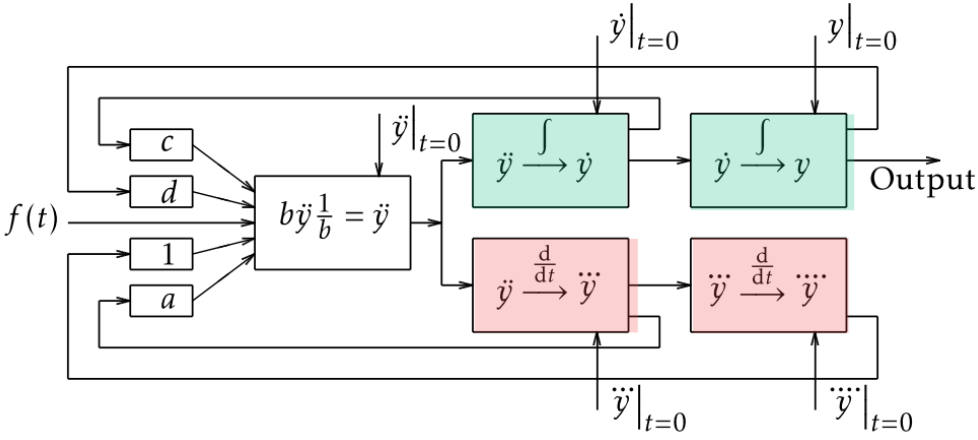


Fig. 6. Solution of a differential equation of fourth degree y""+ay'"+by"+cy'+dy=f(t) for a time dependent signal f(t) with a feedback circuit employing two differentiators and two integrators

Functioncal Composition with Basic Cells

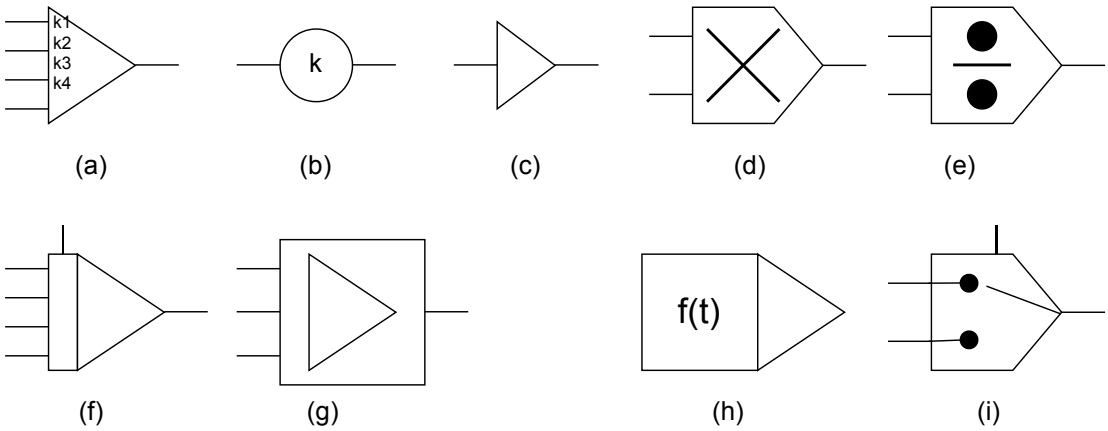


Fig. 7. Building blocks for analog computers: (a) Negating Summer (b) Scaling (c) Negation (d) Multiplier (e) Divider (f) Integrator (g) Differentiator (h) Function block (i) Conditional switch

Architectures

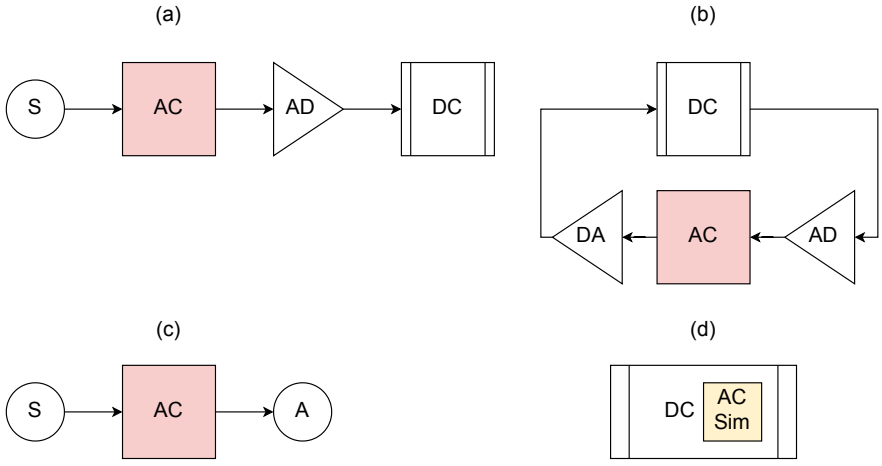


Fig. 8. (a) Analog Computers AC for signal pre-processing connected to Digital Computers DC (b) Analog Computers as Co-processors for Digital Computers (c) Standalone Analog Computers (d) Simulated Analog Computers

Operational Amplifier

The elementary cell for holonic construction principle

[http://www.ecircuitcenter.com/Circuits/opmodel1/opmodel1.htm]

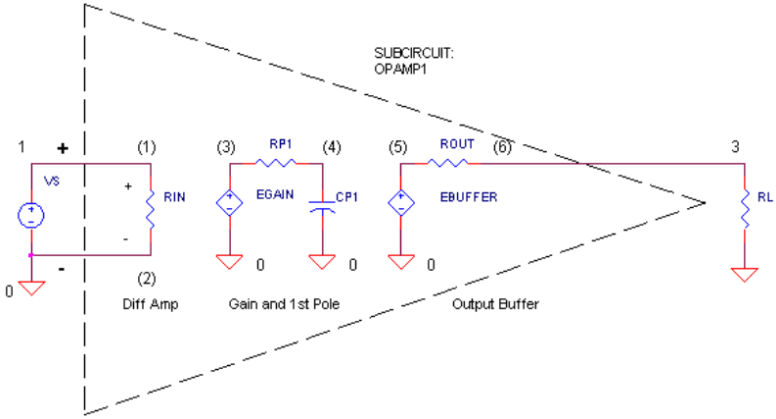


Fig. 9. OPAMP replacement model with voltag sources

Operational Amplifier: Basic Circuits

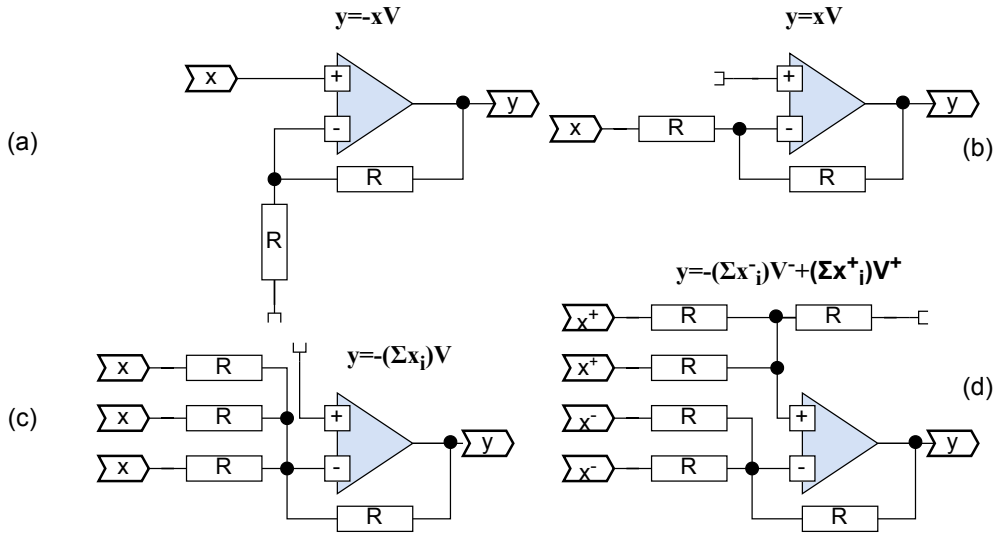


Fig. 10. "Stateless" Circuits (a) Inverting Amplifier (b) Non-inverting amplifier (c) Inverting Sum Amplifier (d) Difference Amplifier / Universal summing amplifier

Operational Amplifier: Basic Circuits

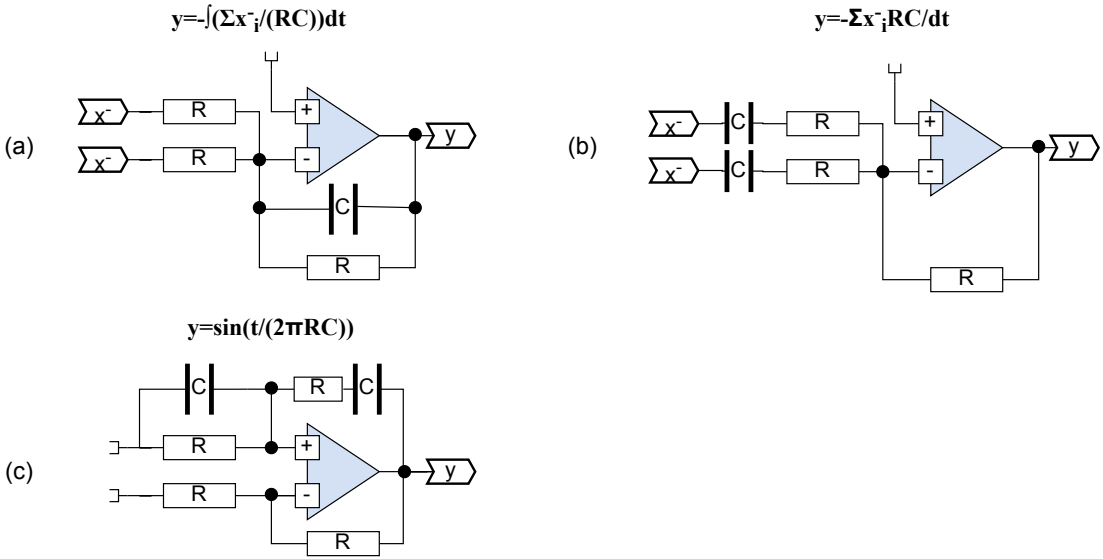


Fig. 11. "Statefull" Circuits (a) Summing Integrator (b) Summing Differentiator (c) Oscillator

Operational Amplifier: Basic Circuits

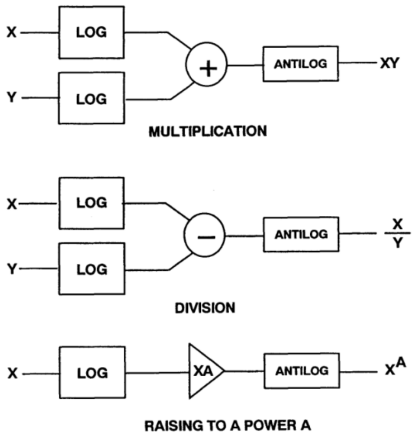


Fig. 12. More arithmetic circuits with non-linear element

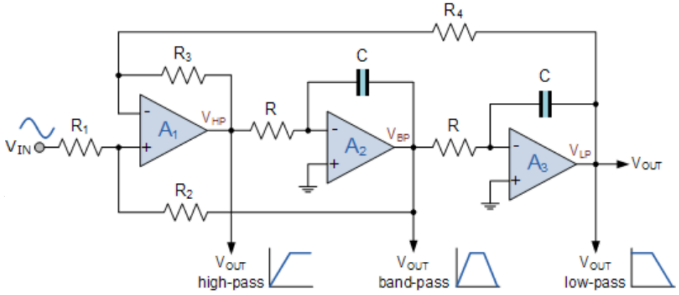


Fig. 13. Frequency domain operation (State Variable Filter Circuit)

Mathematics versa Reality

Real OPAMPs have a lot of deviations from the ideal mathematical OPAMP with different criticality levels:

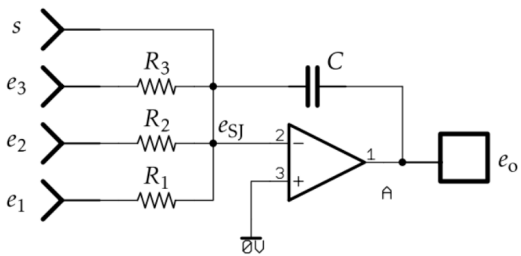
1. Limited open-loop gain (can be low as 50!) ⇒ criticality=middle
2. Limited frequency bandwidth ⇒ criticality=low
3. Non-linearity ⇒ criticality=middle
4. Drift, leakage currents (from output to input) and bias offsets ⇒ criticality=high
5. Temperature dependent transfer function ⇒ criticality=high
6. Clipping (output voltage limited by supply voltage) ⇒ criticality=high
7. Supply voltage dependent transfer function ⇒ criticality=middle
8. Noise ⇒ criticality=low-middle

Mathematics versa Reality

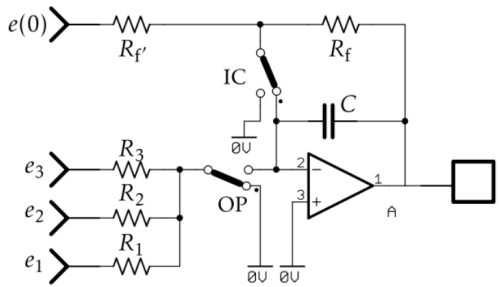
If we want to perform calculations on stationary (DC) signals, some circuits need additional circuitry to deal with the deviations from the ideal OPAMP model.

An integrator which is useless without control logic due to drift and leakage ...

Ideal Circuit



With Control Circuitry



Artificial Neural Networks

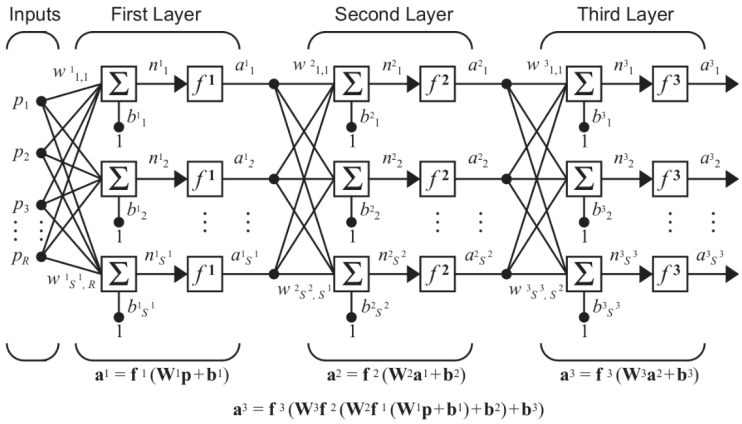


Fig. 14. ANN with three layers

Artificial Neural Networks

Mathematical Model

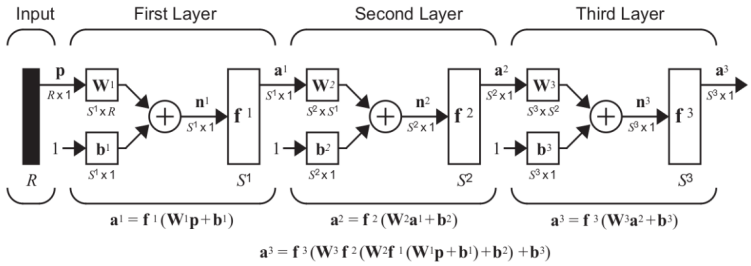


Fig. 15. ANN with three layers and matrix algebra calculations (digital model)

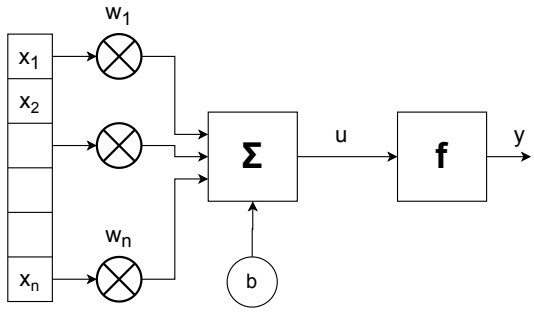
The Perceptron

$$a(\vec{x}) = f(u(\vec{x}) + b)$$

$$u(\vec{x}, \vec{w}) = \sum_{i=1}^{n} x_i w_i$$

$$f(u) = \frac{1}{1 + e^{-u}}$$

$$\vec{P} = \vec{W} = (w_1, .., w_n, b)$$



- The preceptron function *a* consists of two functions:
  - *u*: linear weighted summation
  - *f*(*u*): linear or non-linear activation (transfer) function
  - weights can be negative, zero, or positive
  - output from *u* is not limited
  - output from *f* can be limited

The Perceptron

From digital to analog:

Linear Weighted Summation

Just a summing amplifier. But wait, there is something more to talk about. Discussed next ...

Activation Function

It depends. The ReLu function can be approximated with a diode-based circuit, a sigmoid function (as used in this work) basing on exponential functions can be approximated with a non-linear component, e.g., a bipolar or junction FET transistor (in non-linear range). Other functions like tanh are difficult to be implemented with only a few electronic components.

Minimal Operational Amplifier Circuit OPAMP3

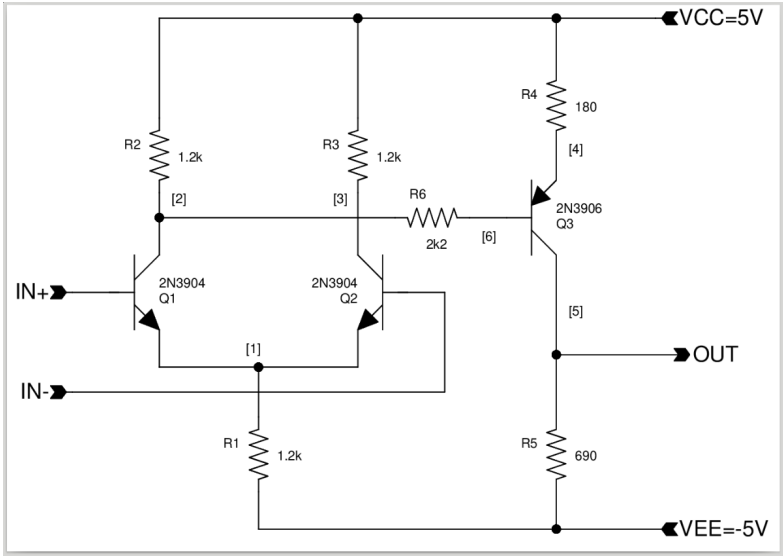


Fig. 16. A minimal OPAMP circuit consisting of a differential and current amplifier requiring only three bipolar transistors. Output swing is asymmetric and about 75% VCC/VEE

Minimal Sigmoid Function Circuit SIGMOID3

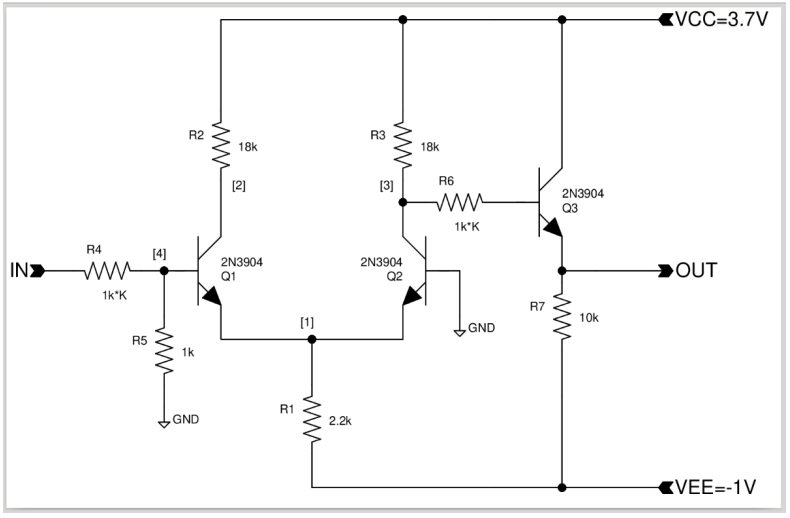


Fig. 17. A minimal sigmoid circuit consisting of a single differential and current amplifier with unity gain requiring only three bipolar transistors. Output voltages are in the range [0,3V]

Minimal Sigmoid Function Circuit SIGMOID3

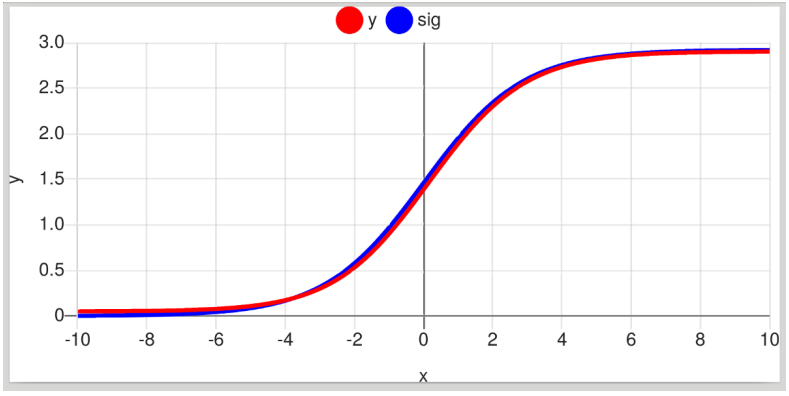


Fig. 18. The sigmoid three-transistor circuit has different x- and y-scaling compared with the mathematical function, but conforms with high accuracy to the scaled mathematical function.The x-scaling can be set by the input resistor multiplication factor *k*. The y-scale is always approximately in the value range [0.05V,2.9V]. The SIGMOID3 circuit needs a slightly odd power supply [-1V,3.7V]

Perceptron Circuit

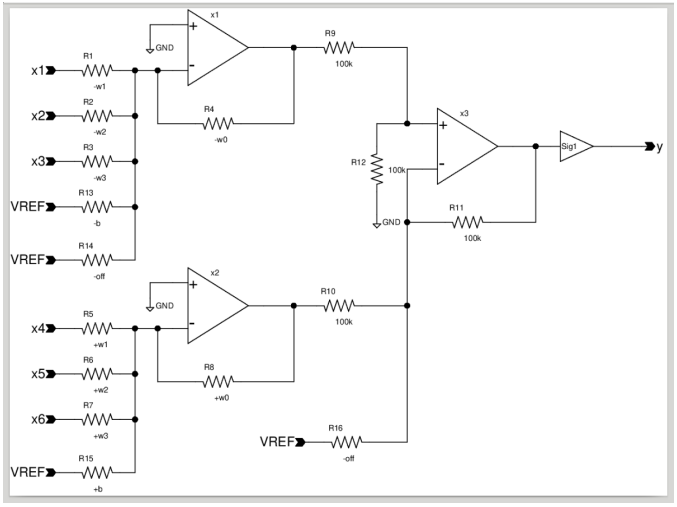


Fig. 19. Single perceptron (neuron) circuit using one OPAMP3 circuit for all negative weights and negative bias, one OPAMP3 circuit for positive weights and positive bias (mutual exclusive), one difference OPAMP3 circuit combining both temporary outputs, and finally applying the sigmoid function with the SIGMOID3 circuit.

Perceptron Circuit

- The weights are independent amplification factors that can be negative or positive.

We cannot use the full summation circuit. The negative weights can be adjusted independently, but the gains of the positive branch weights are linearly dependent making the design process a mess and highly challenging.

- Therefore, we use always inverting summing amplifiers with a final difference amplifier (unity gain) to combine the positive and negative weights branches (and to invert the polarity of the "positive" weights)
- But OPAMP3 differs from real and much more from ideal OPAMPs, and amplification computations from weights requires corrections and the maximal weight is limited (about $w=G_{max}=50$).

The Design Process

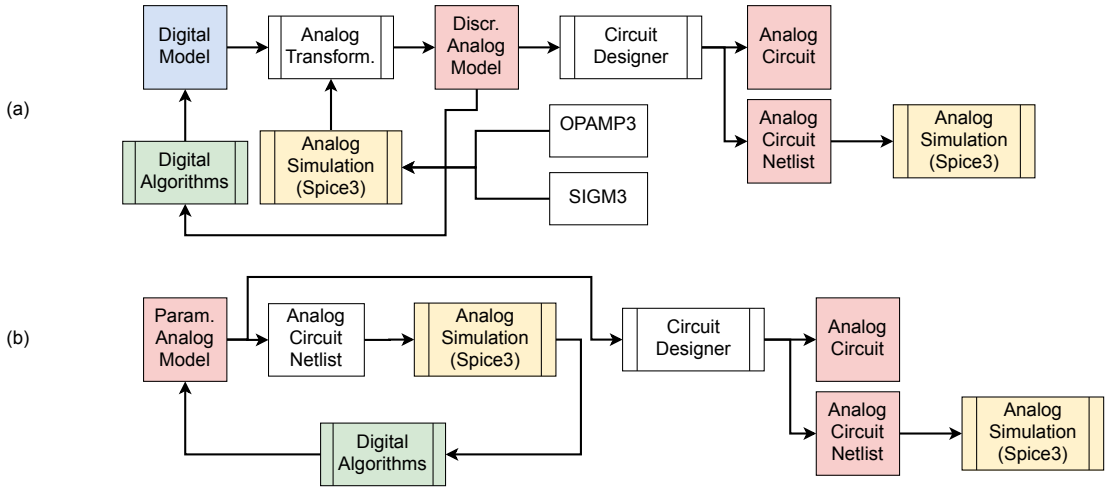


Fig. 20. (a) Indirect synthesis with digital-analog model transformation (b) Direct synthesis and analog model design with simulation-in-the-loop

The Design Process

In this presentation only methodology (a) will be used. It is expected that the analog simulation is close to a hardware implementation using models for real components.

- We have to capture the OPAMP clipping, i.e., the limited output voltage and the maximal gain that can be achieved, and finally a relevant input resistance that affects the total gain.

This is only possible if we use a modified digital ANN model including these analog limitations.

The modified Digital ANN Model (1)

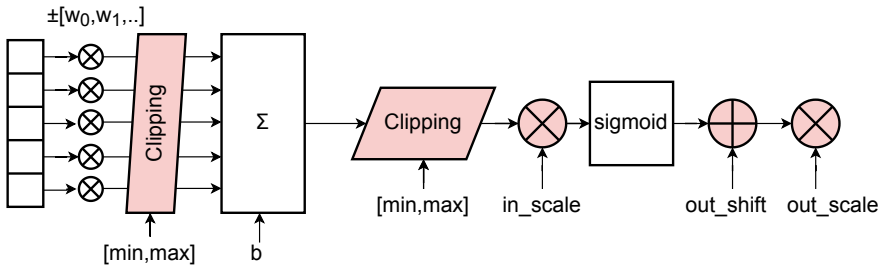


Fig. 21. Modified digital neuron model with combined negative and positive weight paths. The weights as well as the intermediate values are clipped. Finally, the activation function must be scaled according to the analog version.

The modified Digital ANN Model (2)

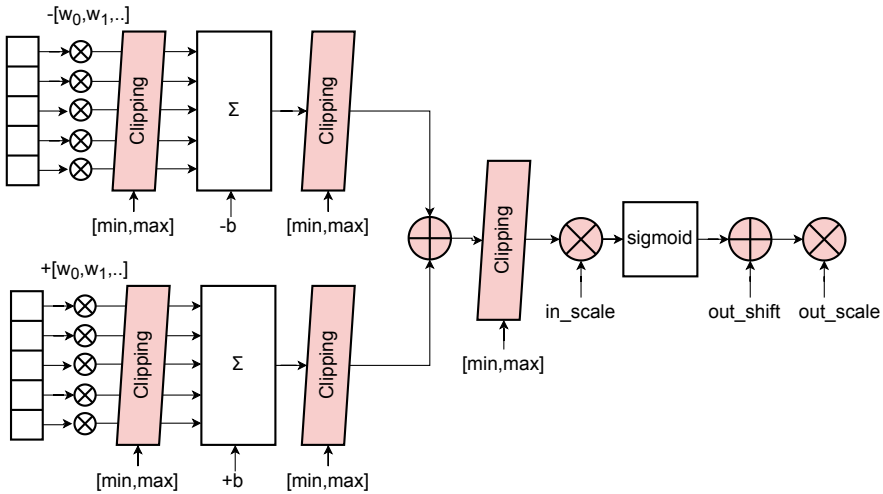


Fig. 22. Modified digital neuron model with separate negative and positive weight paths

We are using and modified the ConvNetJS software framework to implement the modified digital model

Experiments

Benchmark IRIS dataset

- Task: Classification of flowers (sub-species)
- Four numerical input variables (geometrical sizes)
- One categorical output variable (three classes)
- Two classes are linearly separable, one only non-linear
- 151 example instances

The model

- Fully connected ANN with a [4,3,3] layer structure.
- The first input layer is a dummy layer and not included in the analog model
- All neurons uses (modified) sigmoid functions
- The summer clipping was set to 10 (± 10V), the weight clipping was set to 5.

Experiments

Analog Circuit

- SPICE3 model with 2N3904/2N3906 transistor models
- 15 OPAMP3 circuits, 9 SIGMOID3 circuits
- 72 transistors
- 76 external resistors, 6*15+9*9=171 internal resistors, total 247
- Power supply: VCC=15V, VEE=-10V

Experiments

Classification Results

```
              Prediction
              C     A     B
Reference  C  50    0     0
           A  0     51    0
           B  4     0     46

N  : [50,51,50] (151)
TP : [50,51,46] (147)
TN : [97,100,101] (298)
FP : [4,0,0] (4)
FN : [0,0,4] (4)
Unique    : [C,A,B]
Error     : [0.00,0.00,0.08] (0.03)
Accuracy  : [1.00,1.00,0.92] (0.97)
Precision : [0.93,1.00,1.00] (0.97)
Recall    : [1.00,1.00,0.92] (0.97)
F1 Score  : [0.96,1.00,0.96] (0.97)
-----------------------------------
Digital Model
```

```
              Prediction
              C     A     B
Reference  C  50    0     0
           A  0     51    0
           B  15    0     35

N  : [50,51,50] (151)
TP : [50,51,35] (136)
TN : [86,100,101] (287)
FP : [15,0,0] (15)
FN : [0,0,15] (15)
Unique    : [C,A,B]
Error     : [0.00,0.00,0.30] (0.10)
Accuracy  : [1.00,1.00,0.70] (0.90)
Precision : [0.77,1.00,1.00] (0.90)
Recall    : [1.00,1.00,0.70] (0.90)
F1 Score  : [0.87,1.00,0.82] (0.90)
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Analog Model (T=27"C)
```

Fig. 23. Comparison of classification results with the digital and analog model

Experiments

Classification Results

```
             Prediction                          Prediction
                C    A     B                        C    A     B
Reference  C 50.00 0.00  0.00          Reference  C 50.00 0.00  0.00
           A  0.00 51.00 0.00                     A  0.00 51.00 0.00
           B 13.00 0.00 37.00                     B 17.00 0.00 33.00

N  : [50,51,50] (151)                  N  : [50,51,50] (151)
TP : [50,51,37] (138)                  TP : [50,51,33] (134)
TN : [88,100,101] (289)                TN : [84,100,101] (285)
FP : [13,0,0] (13)                     FP : [17,0,0] (17)
FN : [0,0,13] (13)                     FN : [0,0,17] (17)
Unique    : [C,A,B]                    Unique    : [C,A,B]
Error     : [0.00,0.00,0.26] (0.09)    Error     : [0.00,0.00,0.34] (0.11)
Accuracy  : [1.00,1.00,0.74] (0.91)    Accuracy  : [1.00,1.00,0.66] (0.89)
Precision : [0.79,1.00,1.00] (0.91)    Precision : [0.75,1.00,1.00] (0.89)
Recall    : [1.00,1.00,0.74] (0.91)    Recall    : [1.00,1.00,0.66] (0.89)
F1 Score  : [0.88,1.00,0.85] (0.91)    F1 Score  : [0.85,1.00,0.80] (0.89)
-------------------------------------  -------------------------------------
Analog Model (T=80°C)                  Analog Model (T=0°C)
```

Fig. 24. Comparison of classification results of the analog model for different temperatures

Conclusions

1. A computational digital model can be transformed into an approximated analog model based on basic cells of an Analog Computer and by using Operational Amplifier technologies.

2. The digital model must be modified to reflect analog electronics limitations (clipping of output voltages and limited amplification).

3. **The loss of precision is acceptable, compared with digital circuits the transistor count is very low.**

4. The approximation of the generic OPAMP and non-linear function blocks (sigmoid) required only 3 bipolar transistors.

5. We showed the suitability of the digital-analog model transformation approach with a simple Artificial Neural Network.

6. The circuit design process (at the end of the flow) requires adaptation due to non-ideal circuit behavior.

Outlook

Next steps

0. Post fine-tuning of the analog model
1. Test of regression models instead of classification (approximation of polynomials of n-th degree as a gold standard case), wrt. accuracy, precision, temperature dependence
2. Replacing bipolar transistors with junction FET, unmodified circuits, test & evaluation
3. Evaluating the deployment of electro-chemical organic transistors, creating and adapting SPICE3 models, developing modified circuits matching these transistor models.
4. Designing circuits for signal pre-processing, e.g., wavelet decomposition, signal hull approximation.
5. Moving towards the analog model centered design flow.
6. **Surrogate Modeling** of analog circuits with ML

Literature

1. B. Ulmann, Analog Computing. Oldenbourg Verlag München, 2013.
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3. D. E. HYNDMAN, Analog and Hybrid Computing. Pergamon Press, 1970.
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5. Vogel, Analog Computer - Eine Einführung.

End.

Thank you for your attention. All questions are welcome!

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Further information can be found here: http://edu-9.de